REMARKS

Claims 1-3, 5-13, and 15-21 are pending. The Examiner's reconsideration of the objections and rejections in view of the amendments and remarks is respectfully requested.

The Specification has been objected to for an informality. The Examiner stated essentially that the title of the invention is not descriptive. The title of invention has been amended to specify a second instruction set. The Examiner's reconsideration of the objection is respectfully requested.

Claim 1 has been objected to. Applicants appreciate the Examiner's suggestion and have amended Claim 1 to clarify that instructions are decoded/predecoded. The Examiner's reconsideration is respectfully requested.

Claims 1-11, 13 and 15-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lavi et al. (USPN 6,453,407) in view of Ito et al. (USPN 5,742,782). The Examiner stated essentially that the combined teachings of Lavi and Ito teach or suggest all the limitations of Claims 1-11, 13 and 15-20.

Claims 1, 11, and 21 are the independent claims.

Claim 1 claims, *inter alia*, "providing a program of instructions comprising a plurality of instructions of the first instruction set and a plurality of instructions of the second instruction set, wherein the plurality of instructions of the first instruction set are decoded by a decoder in an execution pipeline and the plurality of instructions of the second instruction set are predecoded by a compiler." Claim 11 claims, *inter alia*, "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the sequencer controls a plurality of gates connected between a plurality of execution queues for

storing decoded instructions of the first instruction form and the plurality of execution units." Claim 21 claims, *inter alia*, "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the branch unit switches the processor from the first instruction form to the second instruction form in response to a branch instruction of the first instruction form and switches the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form."

Referring to Claim 1; Lavi teaches a CLIW reference instruction is a decoded VLIW instruction word (see col. 9, lines 57-61). Lavi does not teach "providing a program of instructions comprising a plurality of instructions of the first instruction set and a plurality of instructions of the second instruction set, wherein the plurality of instructions of the first instruction set are decoded by a decoder in an execution pipeline and the plurality of instructions of the second instruction set are predecoded by a compiler" as claimed in Claim 1. Lavi teaches a single instruction set stored as decoded and undecoded instructions. Decoded and undecoded instructions of the same instruction set are not analogous to a first instruction set and a second instruction set, essentially as claimed in Claim 1. For example, Lavi's single instruction set is stored as both regular instructions and CLIW-reference instructions (see col. 16, lines 9-12); Lavi does not teach or suggest instructions and decoded instructions are from different instruction sets. Thus, Lavi fails to teach or suggest "providing a program of instructions comprising a plurality of instructions of the first instruction set and a plurality of instructions of the second instruction set, wherein the plurality of instructions of the first instruction set are decoded by a decoder in an execution pipeline and the plurality of instructions of the second instruction set are predecoded by a compiler" as claimed in Claim 1.

Ito teaches that a decoder includes an instruction buffer (see Figure 3). Ito does not teach or suggest "providing a program of instructions comprising a plurality of instructions of the first instruction set and a plurality of instructions of the second instruction set, wherein the plurality of instructions of the first instruction set are decoded by a decoder in an execution pipeline and the plurality of instructions of the second instruction set are predecoded by a compiler" as claimed in Claim 1. Ito teaches decoding a single instruction set. Therefore, Ito fails to cure the deficiencies of Lavi.

The combined teachings of Lavi and Ito fail to teach or suggest, "providing a program of instructions comprising a plurality of instructions of the first instruction set and a plurality of instructions of the second instruction set, wherein the plurality of instructions of the first instruction set are decoded by a decoder in an execution pipeline and the plurality of instructions of the second instruction set are predecoded by a compiler" as claimed in Claim 1.

Referring to Claim 11; Lavi teaches a CLIW reference instruction is discriminated from a regular instruction by an instruction decoder (see col. 10, lines 1-13). Lavi does not teach "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units" as claimed in Claim 11. Lavi teaches that information that will be read from the CLIW array is fetched according to a CLIW reference instruction - the CLIW reference instruction is fetched from the same pathway as regular instructions. Thus, Lavi fails to teach or suggest de-gating a plurality of execution queues storing the plurality of instructions of the first instruction form. The normal instructions and the reference instructions are fetched along the same pathway (see col. 5, lines 13-21) – thus de-gating the normal

instructions would also de-gate the reference instructions. Accordingly, Lavi fails to teach or suggest "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units" as claimed in Claim 11.

Ito teaches that a decoder includes an instruction buffer (see Figure 3). Ito does not teach or suggest "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units" as claimed in Claim 11. Ito teaches that an instruction buffer stores instructions prior to decoding. Thus, at the very least, the instruction buffer of Ito is not an execution queue – the instructions stored in Ito's instruction buffers cannot be executed because they have not yet been decoded. One of ordinary skill in the art would understand that an execution queue stores decoded instructions. Further, it is clear that the instruction buffer is not de-gated as only one instruction buffer is provided. De-gating the instruction buffer of Ito would terminate an executing program. Therefore, Ito fails to cure the deficiencies of Lavi.

The combined teachings of Lavi and Ito fail to teach or suggest, "de-gating a plurality of execution queues storing the plurality of instructions of the first instruction form, and pausing a fetching of the first instruction form from a memory" as claimed in Claim 11.

Referring to Claim 21; Lavi teaches teaches a CLIW reference instruction is discriminated from a regular instruction by an instruction decoder (see col. 10, lines 1-13). Lavi does not teach or suggest "Claim 21 claims, *inter alia*, "a branch unit connected to an instruction fetch unit for

the first instruction form and a sequencer for the second instruction form, wherein the branch unit switches the processor from the first instruction form to the second instruction form in response to a branch instruction of the first instruction form and switches the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form" as claimed in Claim 21. Lavi teaches that information that will be read from the CLIW array is fetched according to a CLIW reference instruction - the CLIW reference instruction is fetched from the same pathway as regular instructions (see col. 5, lines 13-21). Thus, Lavi fails to teach or suggest switching "the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form" as claimed in Claim 21. The normal instructions and the reference instructions are fetched along the same pathway; Lavi has no need for a branch instruction back to the normal instructions because they are fetched along the same pathway as the reference instructions. Accordingly, Lavi fails to teach or suggest all the limitations of Claim 21.

Ito teaches that a decoder includes an instruction buffer (see Figure 3). Ito does not teach or suggest switching "the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form" as claimed in Claim 21. Ito teaches a single instruction form being decoded by an instruction decoder. Thus, Ito fails to cur the deficiencies of Lavi.

The combined teachings of Lavi and Ito fail to teach or suggest switching "the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form" as claimed in Claim 21.

Claims 5-9 depend from Claim 1. Claims 13 and 16-20 depend from Claim 11. The dependent claims are believed to be allowable for at least the reasons given for Claims 1 and 11,

respectively. Claim 4 was previously cancelled. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 12 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, in view of Ball and Larus, "Efficient Path Profiling," 1996. The examiner stated essentially that the combined teachings of Parady and Ball teach or suggest all the limitations of claim 12.

Claim 12 depends from claim 11. Claim 12 is believed to be allowable for at least the reasons given for claim 11. The Examiner's reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including claims 1-3, 5-13, and 15-21, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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